REMARKS

Applicant thanks the Examiner for the thorough consideration given the present application. Claims 1-13 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the amendments and remarks as set forth below.

Art Rejections

Claims 10-13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Iwazaki (U.S. Patent 6,073,244). Claims 1-5 stand rejected under 35 U.S.C. § 103(a) as being obvious over Velasco et al. (U.S. Patent 6,813,674 – hereinafter "Velasco") in view of Iwazaki. Claims 1-5 and 7-10 stand rejected under 35 U.S.C. § 103(a) as being obvious over Iwazaki. Claim 6 stands rejected under 35 U.S.C. § 103(a) as being obvious over Iwazaki in view of O'Brien (U.S. Patent 5,596,756). These rejections are respectfully traversed.

The independent claims 1 and 7 have been amended to clearly recite that the performance control chip disclosed in the invention is applied to **redeploy whole system resource shared by all said devices by comparing the operating state of each said device.** And the claim 10 has been amended to clearly recite the steps of **ascertaining operating states of all said devices, comparing the operating states of all said devices, and redeploying whole system resource shared by all said devices**.

The support for amendment could be found in the paragraph [0017] of the present invention as:

> "As to the performance control chip 28 is **connected separately to each device** on the motherboard 10, to **compare the operating state of each device** according to the flow rate provided by the performance monitor means 26. Then, the performance control chip 28 can **redeploy the system source**

shared by each device, to adjust the operating rate of each device for promoting the whole system performance of the motherboard 10."

Applicant submits that none of the references nor any combination thereof provide these features. Accordingly, Applicant submits that the independent claims are allowable over the various references.

It is noted that the present invention has the advantage of real-time monitoring and adjusting the operating rate of each device on the motherboard to **redeploy the whole system source to obtain the most efficient performance** of the motherboard. Actually, in the present invention, almost all the devices on the motherboard, including **the CPU 12, the north bridge chip 14, the south bridge chip 16, the AGP slot 20, the PCI slot 22 and the power supply 24**, are monitored by the individual performance monitor means 26 and operated with the specific system source selected by the performance control chip 28.

On the contrary, the devices on the motherboard disclosed by Iwazaki are only divided to two types, one is the CPU, the other is the peripheral processing unit. As illustrated in FIG. 5 of Iwazaki, both the peripheral processing unit 31 and 32 receive the clock signal from the clock generating unit 1 via the signal wire 61, and the CPU 2 receives another clock signal from the clock generating unit 1A via the signal wire 62. That means the peripheral processing units 31 and 32 are regarded as an individual relative to the CPU, and cannot be monitored or adjusted separately. In other words, Iwazaki does not disclose that comparing the operating state of each device on the motherboard to redeploy the whole system resource shared by those devices.

Further, Iwazaki does not disclose that the default configurations stored in the register of the north bridge chip and the south bridge chip could be readjusted to change the priority of each device to share the system source. On the contrary, in the present invention, the configurations stored in the register are dynamic to indicate the real-time priority of each device. Referring to the paragraph [0020] of the present invention, it recites:

> Besides, the performance control chip 28 can also send control signals to the north bridge chip 14 or the south bridge chip 16, **to alter default configurations stored in the register of the north bridge chip 14 or the south bridge chip 16, for readjusting the priority of each device to share the system source**. Generally, according to the default configurations set at the time the motherboard is manufactured, the priority of the device to share the system source has the sequence of CPU (1st) → AGP card (2nd) → peripheral devices mounted on the PCI slots (3rd). However, by introducing the apparatus for adjusting the system performance disclosed by the present invention, the sequence of the priority to share the system source can be readjusted according to the flow rates of the devices measured by the performance monitor means 26. For instance, when the AGP card is busy and the CPU is not busy, the performance control chip 28 will promote the priority of the AGP device, thereby providing more system source for the AGP device.

Thus, Applicant submits that claim 1 is allowable since it is not obvious over the Iwazaki reference to redeploy the systems resources by comparing the operating state of each device. Applicant submits that Iwazaki and the other references do not teach this feature and that, accordingly, claim 1 would not be obvious thereover.

Likewise, Applicant submits that claim 1 would not be obvious over Velasco in view of Iwazaki. The Examiner admits that Velasco does not teach the performance monitor means for monitoring the operating state according to the flow rate of data. The Examiner relies on Iwazaki to show this feature. Accordingly, Applicant submits that the

combination of Velasco and Iwazaki does not render claim 1 obvious for the same reasons recited above.

Applicant further submits that claim 7 is not obvious over Iwazaki since it also now includes the same system relating to the redeploying of system resources by comparing the operating state of each device. Applicant submits that claim 7 is likewise allowable for the same reasons recited above in regard to claim 1.

Claim 10 is an independent method claim which corresponds to apparatus claims 1 and 7. Claim 10 describes the steps of ascertaining the operating states of all devices, comparing the operating states of all devices, and redeploying all system resources shared by the devices. Applicant submits that these steps are also not shown by Iwazaki. Accordingly, Applicant submits that claim 10 is likewise allowable.

Claims 2-6 depend from independent claim 1 and, as such, are also considered to be allowable. Likewise, claims 8 and 9 depend from allowable independent claim 7, and claims 11-13 depend from allowable independent claim 10. All of these claims are allowable based on their dependency from allowable independent claims and further include additional limitations which would make them additionally allowable.

In regard to claim 6, the Examiner relies on O'Brien to teach that the performance control chip is connected to the motherboard power supply. Applicant submits that even if O'Brien does teach this feature, claim 6 remains allowable based on its dependency from allowable claim 1.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejections and allowance of all of the claims are respectfully requested.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned, at the telephone number below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: April 30, 2007

Respectfully submitted,

By _____
Joe McKinney Muncy
Registration No.: 32,334
ROBERT F. GNUSE
Registration # 27296

BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road, Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant